AMENDMENTS TO THE SPECIFICATION

IN THE TITLE:

Please amend the title as follows:

PROCESSOR POWER STATE ~~TRANSISTIONS~~ TRANSITIONS USING SEPARATE LOGIC CONTROL

Please replace the following paragraphs:

IN THE BRIEF DESCRIPTION OF THE DRAWINGS

Page 9, line 7 to page 9, line 9:

~~Figure 4 is~~ Figures 4a-4d are a schematic of the programmable logic device (PLD) used to control power state transitions.

~~Figure 5 is~~ Figures 5a-5b are a timing diagram of signals related to the PLD counter.

IN THE DETAILED DESCRIPTION OF THE PREFERRED EMBODIENT

Page 11, line 1 to page 11, line 7:

Now referring to ~~Figure 4~~ Figures 4a-4d, illustrated is a schematic diagram of the PLD. The PLD controls the timing and reset condition to and from the processor to allow the processor to enter C3 or deep sleep state in order to force an operating mode transition. The PLD sends control signals to the processor to initiate a transition to and back from the C3 state. The control signals may be passed from a chipset controller or are initiated by the PLD. The PLD relies on various latches, clock cycles, and a counter to control transition signals to the processor.

Page 12, line 27 to page 12, line 29:

Now referring to ~~Figure 5~~ Figures 5a-5b, a timing diagram is shown relating PLD control signals with counter 200 outputs CNT[0], CNT[1], CNT[2]. The counter provides sufficient time to perform performance mode transitions.

Page 13, line 1 to page 13, line 10:

Referring back to ~~Figure 4~~ Figures 4a-4d, Latch 250 and latch 255 delay the initiation of counter 200 for a minimum of one SUSCLK period after CPURST-goes inactive.

Referring back to ~~Figure 5~~ Figures 5a-5b, the CPUSLP-signal will be asserted on the rising edge of SUSCLK with the counter output equal to a value of 1. This provides sufficient delay, the minimum being 3 SUSCLK cycles, for the processor to achieve the Stop Grant state and eliminates the need to monitor a system bus for the Stop Grant Acknowledge bus cycle before asserting the CPUSLP-signal to the processor. This puts the processor into the Sleep state. One SUSCLK cycle later the CPU_STP-signal will cause the processor clock to be stopped which forces the processor into the C3 state.

Page 13, line 19 to page 13, line 26:

Referring back to ~~Figure 4~~ Figures 4a-4d, the true and compliment values of CNT2, CNT1, and CNT0 are passed through to comparator 205. From comparator 205 the values are passed through OR gate 206 and the value is stored in latch 215. The output of latch 215 is the signal S_SLP. S_SLP and CPU_SLP (processor sleep signal) are input into logical AND gate 260. The output signal of logical AND gate 260 is C_CPUSLP. The compliment of the value from latch 220 and the signal CPUSTP are input into logical AND gate 265. The output of logical AND gate 265 is the signal CK_CPUSTP.